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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,141	11/20/2003	Seung Ki Joo	069457.0112	8971

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,141	JOO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/055,693.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 16 is objected to because of the following informalities: In line 2 of the claim "AI" should be replaced with "Al". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 10, and 12-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Makita et al. (U.S. Patent No. 6,770,515) in view of Edwards et al. (U.S. Patent No. 5,259,881).

In re claim 1, Makita et al. disclose the method of fabricating a semiconductor device including a crystalline active layer crystallized by performing thermal annealing to an amorphous silicon layer, characterized in that:

the thermal annealing process for crystallizing the amorphous silicon layer (see column 14, line 46 through column 15, line 48) is consecutively performed after a process of depositing a MIC source metal (see column 14, lines 10-45) onto the amorphous silicon layer and before a second material deposition process.

Makita does not disclose the method wherein the MIC source deposition and the thermal annealing process and the crystallizing process are formed within one equipment. Edward et al. disclose the method of deposition and annealing within one piece of equipment (see column 5, line 40 through column 6, line 40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the deposition and annealing of Makita et al. in one piece of equipment, because as Edwards et al. teach, the method prevents contamination.

In re claims 2-5, Makita et al. disclose the method wherein the second material deposition process is a process of depositing a wiring metal layer onto the active layer (see column 18, line 10-25), a process of forming an insulating layer for forming contact holes (see column 17, line 60 through column 18, line 10), a process of forming a gate insulating film and a gate electrode (see column 16, line 60 through column 17, line 20), or a process of forming a gate electrode (see column 17, lines 15-20). The examiner notes that the MIC and annealing process is performed prior to the step of forming the gate insulating layer, the gate, the insulating layer for forming the contact holes, and the wiring layer.

In re claim 10, Makita et al. disclose the method wherein a temperature during the thermal annealing process is 300 °C or higher (see column 14, line 46 through column 15, line 47).

In re claim 12, with respect to claims 1-5, Makita et al. disclose the method further comprising an additional thermal annealing process for improving crystallization of the active layer (see column 15, lines 20-47).

In re claim 13, Makita et al. disclose the method wherein the MIC source metal is used for the wiring metal layer. Makita et al. disclose the metal for the wiring layer (118, See column 18, lines 19-24) is aluminum and disclose the catalyst metal may also be aluminum (see column 8, lines 34-45).

In re claims 14 and 15, Makita et al. disclose the method of forming a silicon oxide film by the plasma CVD method or by the low-pressure CVD method or the atmospheric pressure CVD method of which the conditions (as explained in column 16, line 62 through column 17) include the method wherein a substrate of the semiconductor device is heating during the process of forming the insulating layer (see column 17, line 60 through column 18, line 8, and column 16, line 62 through column 17, line 7 for conditions of the deposition), a temperature that is lower than the thermal annealing temperature of the active layer (see column 14, line 46 through column 15, line 47).

In re claim 16, Makita et al. disclose the method wherein at least one material selected form a group consisting of Ni, pd, Ti, Ag, Au, Al., Sn, Sb, Cu, Co, Cr, Mo, Tr, Ru, Rh, Cd, Pt, or a combination thereof is used as the MIC source metal (104, see colum8, lines 34-45).

In re claim 17, with respect to claims 1-5, Makita et al. disclose the method wherein the semiconductor device is a thin film transistor (see abstract).

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makita et al. (U.S. Patent No. 6,770,515) and Edwards et al. (U.S. Patent No. 5,259,881) in view of Fonash et al. (U.S. Patent No. 5,994,164).

Makita et al. and Edwards et al. disclose the method as claimed and rejected above, but do not disclose the method wherein the substrate is heated during the process of applying the MIC source metal at a temperature of 200 °C or higher. Fonash et al. disclose the method of depositing a catalyst metal by an evaporation technique at a temperature of 200 °C or higher (see Example 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the metal by this method because it is a method that allows for larger grain size and selectively controlling the grain size of the crystalline films which is desirable in TFT devices.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makita et al. (U.S. Patent No. 6,770,515) and Edwards et al. (U.S. Patent No. 5,259,881) in view of Jang et al. (U.S. Patent No. 6,309,951).

Makita et al. and Edwards et al disclose the method as claimed and rejected above, but do not disclose the method wherein the thermal annealing process is performed under vacuum.

Jang et al. disclose the method of performing the annealing of the amorphous silicon under vacuum (see column 5, lines 3-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the layer of Makita

et al. under vacuum, as in the system of Edwards et al., because it allows for reduction of contamination.

The examiner notes that Applicant does not teach that the pressure range solves any stated problem or is for any particular purpose. Therefore, the pressure range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the annealing at the pressure range of 10 to 1.0 x 10 – 10 Torr, since the invention would perform equally well when the annealing occurs at different pressures within the vacuum range to improve crystallization and reduce contamination, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makita et al. (U.S. Patent No. 6,770,515) and Edwards et al. (U.S. Patent No. 5,259,881) in view of Seo et al. (U.S. Patent No. 6,306,692).

Makita et al. and Edwards et al disclose the method as claimed and rejected above, but do not disclose the method of implanting impurities into the active layer before the thermal annealing process of the active layer and being characterized in that the impurities are activated during the thermal annealing of the active layer.

Seo et al. disclose the method of implanting impurities into the active layer before the thermal annealing process of the active layer and being characterized in that the impurities are activated during the thermal annealing of the active layer (see column 4, lines 5-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implant impurities into the active layer before the thermal annealing process of the active layer because the method of Seo et al. activates the impurities and crystallizes the amorphous silicon in one annealing step which reduces the number of process steps of Makita et al. The examiner notes that Makita et al. disclose annealing to crystallize, doping with impurities and then annealing again to activate the impurities.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk